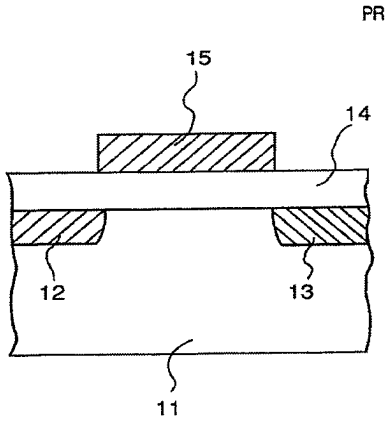
REMARKS

The non-final Office Action dated August 5, 2010, indicated the following rejections under 35 U.S.C. § 103(a): claims 1-7, 9-20, 30-37, 39 and 43-45 stand rejected over Akimoto *et al.* (US 2002/0117689) in view of Baba *et al.* (U.S. 5,686,739) and Yee *et al.* (U.S. 5,736,890); claim 8 stand rejected over the '689, '739, and '890 references, and further in view of Baba (US 5,589,696); and claims 21-29 stand rejected over Mizutani *et al.* (U.S. 5,616,944) in view of the '696 and '890 references. Applicant respectfully traverses each of the rejections, and in the discussion set forth below, does not acquiesce to any rejection or averment in this Office Action or the Office Action(s) of record unless Applicant expressly indicates otherwise. Applicant further notes that, despite the instant rejections involving a new combination of references, various rejections appear to again rely upon assertions as previously made. As such, Applicant fully incorporates its traversals of records herein.

Applicant respectfully traverses the § 103 rejections of claims 1-20, 30-37, 39 and 43-45, each of which relies upon the '739 reference, because the '739 reference (as combined) lacks correspondence. For example, the cited portion of the '739 reference neither discloses claim limitations as asserted nor teaches the claimed invention "as a whole" (§ 103(a)), including aspects regarding, *e.g.*, a control circuit configured to apply a control signal to a reverse-biased body change "a concentration of carriers in a portion of the intermediate region extending from the second junction and offset from the first junction," as in claim 1 and also relevant to other independent claims. As another example, the cited portion of the '739 reference does not disclose, teach or suggest a control circuit configured to apply a control signal to switch "to a current-conducting state in which the first body is in an avalanche breakdown condition and current passes between the data storage node and the first body," as in independent claim 30 and also relevant to independent claims 32, 38, 39, 43 and 45. As yet another example, the cited portion of the '739 reference does not disclose, teach or suggest a control circuit that applies a control signal "to control the gate, the P-type region and the N-type region to switch between at least two stable conductance states" by presenting "an electric field substantially at only said one of the two junctions" as in independent claim 18. Because the reference does not teach these aspects, no reasonable interpretation of the asserted prior art can provide correspondence. As such, the rejections fail.

The Office Action acknowledges that the '689 reference fails to disclose, teach or suggest the claimed control circuit and its functionality relative to each of the claims, and further asserts that background discussion in the '739 reference discloses these limitations. However, the cited portion of the '739 reference refers to the control of a three-terminal quantum device in which the gate spans both junctions in a source/channel/drain region. Nothing in the cited references or in the Office Action explains how a control circuit applying a signal in accordance with the '739 reference would somehow cause the same response in a completely different device (the primary '689 reference). FIG. 1 of the '739 reference is copied below for convenience:

FIG.1



Referring to the placement of gate 15 above, the described control in the '739 reference requires the generation of an inversion layer spanning the entire channel between the source 12 and drain 13. As stated in the cited portion of the '739 reference, the application of negative and positive threshold voltages to the gate 15 respectively cause "an accumulation layer filled with holes is produced at the bulk surface region under the gate" and "an inversion layer filled with electrons is caused at the bulk surface region under the gate."

Accordingly, the cited device in the '739 reference operates so that the application of either a negative or positive voltage to the gate 15 results in an inversion layer that spans across the entire channel between the source and drain 12 and 13, with respective junctions at the channel/drain region 13 (under negative bias) and at the channel/source region 12 (under positive bias). In neither of these instances is the channel region modulated by "changing a concentration of carriers in a portion ... extending from the second junction and offset from the first junction" as claimed. Any control circuit in combination with the gate 15 in FIG. 1 above and operating as

required in the '739 reference would not appear capable of functioning as claimed, at least because the gate is not offset relative to a junction as in the claimed invention.

Furthermore, as the gate and related control signal applied thereto in FIG. 1 of the '739 reference operate in a breakdown condition in both of the indicated states, the cited portions do not correspond to the claimed control circuits as configured to cause switching between a stable conductance state, and a current-conducting state involving an avalanche breakdown. Similarly, the '739 reference does not appear to disclose any control capable of resulting in a "current-blocking" state as claimed. Referring to claim 18, the proposed combination of references also does not present "an electric field substantially at only said one of the two junctions" to effect modulation of a channel region. Further regarding independent claim 43, the cited portion of the '739 reference also fails to disclose a control circuit configured to apply a control signal to cause an "avalanche breakdown condition occurring in the lower portion of the intermediate region, the upper portion of the intermediate region being arranged to inhibit hot carriers from the lower portion reaching the upper surface in a current-conducting state." No mention is made of any hot carrier inhibition.

In view of the above, the § 103(a) rejections fail to establish correspondence to claims 1-20, 30-37, 39 and 43-45. Applicant therefore requests that the rejections be removed.

Applicant further traverses the rejections of claims 1-20, 30-37, 39 and 43-45 because the cited references teach away from the hypothetical embodiment involving the proposed combination of references. Consistent with the recent *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main reference - the rationale being that the prior art teaches away from such a modification.[1] Applicant submits that the combination would render the hypothetical embodiment (corresponding to the rejection's proposed combination) inoperable due to the creation of an inversion layer across an entire channel.

More specifically, the gate control according to the '739 reference would result in the creation of an inversion layer across the entire channel region. Moreover, this control further involves two states respectively requiring an avalanche breakdown relative to junctions at either

[1] *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.")

the source or drain region. Referring to FIG. 1 above, as discussed in the cited portion of the '739 reference, "[a]s is known, under the reverse bias, the tunneling of carriers is possible in both degenerate and nondegenerate junctions." Accordingly, there is no motivation to combine references as asserted, and the rejections fail.

Applicant also traverses the § 103 rejections of claims 21-29, which rely upon the '696 reference, because the '696 reference (as combined) lacks correspondence. For example, the cited portion of the '696 reference neither discloses claim limitations as asserted nor teaches the claimed invention "as a whole" (§ 103(a)), including aspects regarding, *e.g.*, a control circuit configured to apply a control signal to a body (when the body is reversed biased) "to present an electric field substantially at only one of the first and second junctions" to cause the body to switch "from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body" as in independent claim 21, and relevant to independent claim 27.

The rejections of claims 21 and 27 rely upon an unsupported opinion regarding what the secondary '696 reference "would" or "could" do, while the cited portions therein make no mention of this alleged functionality. Nowhere in the cited portions (column 3:1-15; column 4:1-15) does the '696 reference mention a control signal that controls the presentation of an electric field to switch a body between a stable state to a conductance state in which an avalanche breakdown condition occurs. In fact, no mention whatsoever is made of such limitations.

Referring to cited Figure 1 of the '696 reference, the gate 21 is over both underlying junctions, and the application of a bias to the gate results in an inversion layer in the entire spacer region between regions 13 and 15 (*see*, *e.g.*, column 3:14-28). The gate 21 thus does not "present an electric field substantially at only one of the two junctions" as asserted.

Referring to cited Figure 2 of the '696 reference, the gate (also labeled 21) applies a bias, not to the channel region between source and drain regions 13/15, but to a third semiconductor layer 27. Referring to column 5:17-40 of the '696 reference, the signal applied to the gate 21 causes a depletion layer in the third semiconductor layer 17. The '696 reference requires that this third semiconductor layer 17 "spans the first and second semiconductor layers 13 and 15" so that "great tunneling current can therefore flow between the first and the second semiconductor

layers 13 and 15 with no hindrance." Nothing in the cited portion of the '696 reference suggests the creation of an avalanche breakdown in the body (11, between 13 and 15) for passing current.

In view of the above, the Office Action has also failed to establish correspondence to the limitations in claims 21-29. Accordingly, Applicant submits that the rejections of claims 21-29 are improper and should be reversed.

Applicant further traverses the rejections of claims 21-29 because the cited references teach away from the hypothetical embodiment involving the proposed combination of references, as consistent with the recent *KSR* decision and M.P.E.P. § 2143.01 as cited above. As applicable here, the proposed combination of references would render the hypothetical embodiment (corresponding to the rejection's proposed combination) inoperable due to the resulting tunneling current through the third semiconductor layer 17, as discussed above. Accordingly, the apparent embodiment as suggested in the Office Action would be inoperable for operating in "a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body." As such, there is no motivation for combining references as asserted, and the rejections of claims 21-29 fail.

Regarding the Examiner's Response to Arguments at page 27, Applicant submits that these comments do not appear relevant as the rejections do not rely upon any assertions made therein. However, Applicant traverses the Office Action's apparent suggestion that the claimed control circuit (*e.g.*, a logic circuit) as configured relates to "method" claim limitations. To the extent that this argument may be applied to the various assertions in the Office Action that the cited references "could" be configured to carry out the functions of the claimed circuit components/controllers, Applicant notes that without citing any correspondence, teaching or suggestion of this functionality in the references themselves, such rejections fail. As Applicant has previously explained, various portions of the M.P.E.P. (and relevant law) support the well-established understanding that functional limitations pertaining to claimed structure (*e.g.*, in the context of a control circuit/logic circuitry) must be given patentable weight. Many thousands of patents have been issued and approved by the U.S.P.T.O. and related authoritative bodies based upon claims in which circuits are defined by their function. One relatively simple example is in the case of an analog to digital converter circuit, which is simply a circuit that converts an analog signal to a digital signal; the functionality of the circuit, not its structure or form, define what the circuit does. Correspondingly, anticipation of a control circuit or logic circuit having

functionality as claimed in accordance with various embodiments is not established by citation to a different circuit for which no corresponding functionality has been defined. Were the Office Action's position regarding circuit configurations (*e.g.*, control circuit configuration) allowed to stand, thousands of issued patents could be rendered invalid in this context. For the reasons outlined below, Applicant believes all of the claims to be allowable. Should the Examiner have any misunderstanding regarding these matters or the arguments presented herein, Applicant encourages the Examiner to telephone the undersigned.

To the extent that the Examiner may be relying upon the assertions made in the Response to Arguments section, Applicant maintains its traversals regarding any improper reliance upon an assertion that "limitations regarding method of operating the device are not given patentable weight," as such an assertion contradicts M.P.E.P. §§ 2143.03, 2173.05(g) and relevant law. Similarly, to the extent that the Examiner may be alleging that the claimed functionality is allegedly inherent, Applicant also maintains its traversals as the Office Action fails to meet the burden of proof for inherency under M.P.E.P. § 2112.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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